cont A'

propagation delay which varies in response to a respective control signal; wherein the first signal generator is coupled to an or each odd amplifier stage in order to apply said first periodic signal as said control signal for the or each odd amplifier stage and the second signal generator is coupled to an or each even amplifier stage in order to apply said second periodic signal as said control signal for the or each even amplifier stage so that the propagation delay through the or each even amplifier stage decreases when the propagation delay through the or each odd amplifier stage increases; and

wherein said first and second signal generators are arranged to generate said first and second periodic signals such that the propagation delay through each of the amplifier stages is modulated about half the period of said first and second periodic signals.

REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on June 6, 2001, and the references cited therewith.

Claims 1-30 are canceled without prejudice or disclaimer, and claims 31-58 are added; as a result, claims 31-58 are now pending in this application. The applicant reserves the right to reintroduce claims 1-30 at a later date. The new claims merely cover other claimable embodiments of the Applicant's invention as supported by the application as originally filed. The new claims do not introduce any new matter. The new claims are similar in scope to the cancelled claims 1-30 and therefore no new search should be required. Applicant respectfully requests reconsideration of the above-identified application in view of the amendments above and the remarks that follow.

On page 7, a correction has been made at line 32 to reduce the expression for the oscillation frequency by a factor of 2. In the frequency divider as illustrated in Figure 2, a portion of the signal must travel twice through each of the latches 10a and 10b before returning to the same point in the circuit because the output of the latch 10b is connected to the inverse input of the latch 10a. Thus, the period of the signal traveling around the frequency divider is $2(T_1 + T_2)$. Applicant submits that this is an obvious error and that this error should be correct by dividing the expression for the oscillation frequency by a factor of 2. This correction has required subsequent corrections at page 7 lines 34 and 35 and page 10 lines 8 and 9. On page 10 at line 12 a clarification has been made to change "frequency $1/2f_{in}$" to "frequency $f_{in}/2$".

Claim Objections

Claims 3-13, 19, 23, 25 and 27-30 are objected to under 37 CFR 1.75(c) as being in improper form because a multiple dependent claim should refer to other claims in the alternative only and/or cannot depend from any other multiple dependent claim (MPEP 608.01(n)).

Claims 3-13, 19, 23, 25 and 27-30 are cancelled. The new claims do not include any multiple dependencies, thereby overcoming the objection under 37 CFR 1.75(c).

§112 Rejection of the Claims

Claims 1-30 were rejected under 35 USC § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claims 1-30 were rejected under 35 USC § 112, first paragraph, because of the technical deficiencies of claims 1, 14 and 20. Claims 6, 12, 14-19, 23-24 and 28-29 were rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

Claims 1 and 20

The Examiner rejected old claims 1 and 20 stating that the specification fails to teach how to make and use the modulation means as recited in these claims.

We disagree with this view. The specification describes, with reference to Figures 1 to 3, a first embodiment of the invention in which a control signal (clk) varies the resistance of clock transistors N3/N4 in order to vary (modulate) the propagation delay through an amplifier stage (see the passage from line 35 of page 8 to line 17 of page 9). The specification also describes, with reference to Figures 4 to 6, a second embodiment in which the control signal (clk) varies the hysteresis of a memory element in an amplifier stage in order to vary (modulate) the propagation delay through the amplifier stage (see the passage from line 18 of page 9 to line 34 of page 10).

In the first embodiment a description of a latch circuit is given with reference to Figure 1 and then a description is given of how two of these latch circuits can be connected in series to

form the frequency divider circuit shown in Figure 2. The latch circuit shown in Figure 1 is therefore acting as one of the amplifier stages of the frequency divider shown in Figure 2. As the Examiner will appreciate, the description of the latch circuits used in the first embodiment are described in detail in the specification, even down to the aspect ratios of the transistors used. Similarly, the latch circuit used in the second embodiment in which the hysteresis of the latch circuit is varied is shown in Figure 6. As the Examiner will see, the description of this latch circuit is also given in detail allowing those skilled in the art to build the latch circuit and hence the frequency divider circuit of the present invention.

With regard to the schematic equivalent diagram shown in Figures 3 and 4, these have been included for explaining how the frequency divider circuits of the first and second embodiments are operating. As the Examiner will appreciate, when dealing with transistor circuits and frequency divider circuits such as in the present case, it is often difficult to understand how the circuits are operating without these schematic equivalent diagrams.

Notwithstanding the above, we have amended the new independent claims in order to try to clarify what was meant by the modulating means and the amended claims now correspond more closely to the wording used in the description (see for example the passage from line 23 of page 6 to line 3 of page 7).

Further, independent claim 31 has been amended so that it is no longer in means plus function format.

Claim 14

The Examiner rejected old claim 14 stating that the specification fails to teach how to make and use the varying means of the latch as recited in claim 14.

Although we respectfully disagree with the Examiner for the reasons set out above for old claims 1 and 20, claim 14 has now been deleted and the newly filed claims 31 to 57 do not contain claims directed to a semiconductor latch.

Claims 2-13, 15-19 and 21-30

The Examiner rejected old claims 2-13 and 21-30 because of the alleged technical

deficiencies of old claims 1 and 20. As explained above, it is respectively submitted that the Examiner's rejection of old claims 1 and 20 is incorrect and therefore the Examiner's rejection of claims 2-13 and 21-30 is also incorrect.

With regard to old claims 15-19, as stated above all claims directed to a semiconductor latch have been deleted from the application.

Claims 6 and 23

The Examiner rejected old claims 6 and 23 stating that the recitation of "said modulating means varies the strength of connection between adjacent amplifiers stages" is indefinite because it is unclear as to how the strength of connection between adjacent amplifier stages is varied by the modulating means.

These claims were directed to the first embodiment in which, as described above, the control signal (clk) varies the resistance of clock transistors N3/N4 in order to vary the propagation delay. This is effectively the same as varying the strength of connection between adjacent amplifier stages.

New claims 35 and 50, which correspond generally to old claims 6 and 23 respectively, specify that each amplifier stage comprises connection logic circuitry and that the control signal is operable to vary the propagation delay through this connection logic circuitry. This amendment has been made purely to clarify the meaning of the original claims.

Claim 12 and 28

The Examiner rejected old claim 12 stating that it is indefinite because it fails to recite the interconnection between the logic means and the amplifier stages, and has rejected old claim 28 stating that it is unclear as to how the logic circuits provide division by ratios other than powers of two.

Claims 12 and 28 relate to the frequency divider illustrated in Figure 8. As shown in Figure 8, a logic circuit is connected in series between amplifier stages L4 and L5 to enable division by a ratio other than a power of two. The way in which this is achieved is described in detail from page 12 line 10 to page 13 line 1 of the application.

New claims 44 and 57 correspond generally to old claims 12 and 28 respectively, but clarify that the logic circuitry is connected in series between at least two of the amplifier stages in order to enable division by ratios other than simple powers of two. This amendment has been made purely to clarify the meaning of the original claims.

Claim 14 to 16 and 19

The Examiner rejected old claims 14 to 16 and 19 stating that it is unclear as to which is the varying means of the latch.

As stated above, all claims directed to the semiconductor latch have been deleted.

Claim 24

The Examiner rejected old claim 24 stating that it is indefinite because it is unclear as to how the hysteresis of the amplifier stages is varied by the modulating step.

We respectfully disagree. This claim relates to the second embodiment of the invention described with reference to Figures 4 to 6. In contrast with the first embodiment, where the strength of connection between the amplifier stages is varied, in this second embodiment the hysteresis of a differential amplifier within each amplifier stage is directly varied. An exemplary circuit of this type is shown on Figure 6. As stated in the description at lines 21 to 34 of page 10:

> "As in the first embodiment, the propagation delay through the latch 60 is dependent upon the time taken to force either Q' or QB' into a logic low. Further, when a high frequency signal is applied to CLK, transistors N3' and N4' do not necessarily have time to become fully open or fully closed, but anyhow react as variable resistances, the values of which fluctuate in response to the input signal (CLK). As a result of this fluctuating resistance, the time taken to force the latch 60 into each different state is modulated and so the propagation delay through the latch 60 is modulated. Therefore, in this embodiment the clock signal is effectively modulating the propagation delay by modulating the hysteresis of the latch circuits."

New claim 53, which corresponds generally to old claim 24, specifies that the respective control signals vary the hysteresis of each of the amplifiers stages. It is submitted that this clearly indicates how the hysteresis of each amplifier stage is varied, bearing in mind the above passage of the description.

Claim 29

The Examiner rejected old claim 29 because it is a mixture of method and apparatus claims. Claim 29 has been deleted.

Claims 17-18

The Examiner rejected old claims 17 and 18 stating they are indefinite due to the technical deficiencies of claim 14.

As stated above, all claims directed to the semiconductor latch have been deleted.

Applicant respectfully disagrees with the rejections of claims under under 35 USC § 112. Nevertheless, Applicant has elected to cancel claims 1-30 solely for the purpose of expediting the patent application process in a manner consistent with the PTO's Patent Business Goals (PBG) 65 Fed. Reg. 54603 (September 8, 2000).

§102 Rejection of the Claims

Claims 1-3 and 20-26 were rejected under 35 USC § 102(b) as being anticipated by Suzuki et al. (US 4,356,411). Claims 14-18 were rejected under 35 USC § 102(b) as being anticipated by Suzuki et al. (US 4,356,411).

Suzuki et al describes a number of flip-flop circuits adapted for use in a counter.

Figure 4 of Suzuki et al shows a circuit diagram of a flip-flop circuit which is utilized as a binary flip-flop where the output data changes at the trailing edge of a clock signal. The circuit shown has two latches in a master-slave configuration and the applied clock signal is a logic signal, i.e. it only has a high state and a low state (see table at lines 34 to 40 of column 7).

As stated at lines 41 to 47 of column 7 of Suzuki et al, the flip-flop illustrated in Figure 4 does **not** use an anti-phase clock signal. The purpose of removing the anti-phase clock signal is

discussed in the passage from line 48 of column 7 to line 2 of column 8 of Suzuki et al and is related to reducing the number of transistors which have to be switched in order for a signal to propagate through the flip-flop.

Figure 5 of Suzuki et al shows a simplified version of the flip-flop illustrated in Figure 4.

Suzuki et al does not describe a frequency divider circuit in which an even number of amplifiers stages are connected in series. Further Suzuki et al does not describe the following features of independent claims 31 and 48:

1. applying a first periodic signal to be frequency divided to the odd amplifier stages such that propagation delay through each odd amplifier stages is varied about half the period of the first periodic signal; and

2. applying a second periodic signal, which is in anti-phase with the first periodic signal, to the even amplifiers such the propagation delay through each of the even amplifier stages is varied about half the period of the second periodic signal, whereby the propagation delay through the odd amplifier stages increases as the propagation delay through the even amplifiers stages decreases.

As stated above, a requirement of independent claims 31 and 48 is that the second periodic signal is in anti-phase with the first periodic signal. As Suzuki et al explicitly discusses advantages in **not** using an anti-phase clock signal, it is submitted that Suzuki et al teaches away from the invention as claimed in claims 31 and 48.

It is therefore submitted that Suzuki et al neither teaches nor suggests the invention as claimed in claims 31 and 48 and therefore are in allowable form.

New claims 32, 33, 49, 52, 50 and 53 to 55, which correspond generally to original claims 2 to 26 respectively, are dependent on either claim 31 or 48 and therefore are also neither taught nor suggested by Suzuki et al and are also now in allowable form.

New claims 34, 35, 37 to 41, 43 to 45, 56 and 57 are dependent claims which correspond generally to old claims 4, 6, 5 to 10, 11 to 13, 27 and 28 respectively. New claims 36, 42, 46, 47 and 51 are new dependent claims directed to features of the first embodiment. All of these claims are dependent on either claim 31 or 48 and therefore are also neither taught nor suggested

by Suzuki et al and are also now in allowable form.

New claim 58 is directed to a radio receiver comprising a frequency divider circuit as claimed in claim 31. As claim 58 includes all the features of claim 31, it is submitted that this claim is neither taught nor suggested by Suzuki et al and is also now in allowable form.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612-349-9592) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

JAMES DIGBY COLLIER ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 349-9592

Date Dec. 6, 2001 By Ann M. McCrackin

Ann M. McCrackin
Reg. No. 42,858

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 6 day of December, 2001.

ANN McCRACKIN
Name

Ann McCrackin
Signature